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Kind regards,

Team Nexperia

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

## 74HC/HCT173

Quad D-type flip-flop; positive-edge trigger; 3-state

Product specification  
File under Integrated Circuits, IC06

December 1990

## Quad D-type flip-flop; positive-edge trigger; 3-state

## 74HC/HCT173

## FEATURES

- Gated input enable for hold (do nothing) mode
- Gated output enable control
- Edge-triggered D-type register
- Asynchronous master reset
- Output capability: bus driver
- I<sub>CC</sub> category: MSI

## GENERAL DESCRIPTION

The 74HC/HCT173 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT173 are 4-bit parallel load registers with clock enable control, 3-state buffered outputs (Q<sub>0</sub> to Q<sub>3</sub>) and master reset (MR).

When the two data enable inputs ( $\overline{E}_1$  and  $\overline{E}_2$ ) are LOW, the data on the D<sub>n</sub> inputs is loaded into the register

synchronously with the LOW-to-HIGH clock (CP) transition. When one or both  $\overline{E}_n$  inputs are HIGH one set-up time prior to the LOW-to-HIGH clock transition, the register will retain the previous data. Data inputs and clock enable inputs are fully edge-triggered and must be stable only one set-up time prior to the LOW-to-HIGH clock transition.

The master reset input (MR) is an active HIGH asynchronous input. When MR is HIGH, all four flip-flops are reset (cleared) independently of any other input condition.

The 3-state output buffers are controlled by a 2-input NOR gate. When both output enable inputs ( $\overline{OE}_1$  and  $\overline{OE}_2$ ) are LOW, the data in the register is presented to the Q<sub>n</sub> outputs. When one or both  $\overline{OE}_n$  inputs are HIGH, the outputs are forced to a high impedance OFF-state. The 3-state output buffers are completely independent of the register operation; the  $\overline{OE}_n$  transition does not affect the clock and reset operations.

## QUICK REFERENCE DATA

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

| SYMBOL                              | PARAMETER                                                         | CONDITIONS                                    | TYPICAL  |          | UNIT     |
|-------------------------------------|-------------------------------------------------------------------|-----------------------------------------------|----------|----------|----------|
|                                     |                                                                   |                                               | HC       | HCT      |          |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>CP to Q <sub>n</sub><br>MR to Q <sub>n</sub> | C <sub>L</sub> = 15 pF; V <sub>CC</sub> = 5 V | 17<br>13 | 17<br>17 | ns<br>ns |
| f <sub>max</sub>                    | maximum clock frequency                                           |                                               | 88       | 88       | MHz      |
| C <sub>I</sub>                      | input capacitance                                                 |                                               | 3.5      | 3.5      | pF       |
| C <sub>PD</sub>                     | power dissipation<br>capacitance per flip-flop                    | notes 1 and 2                                 | 20       | 20       | pF       |

## Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz

f<sub>o</sub> = output frequency in MHz

∑ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

C<sub>L</sub> = output load capacitance in pF

V<sub>CC</sub> = supply voltage in V

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> − 1.5 V

## ORDERING INFORMATION

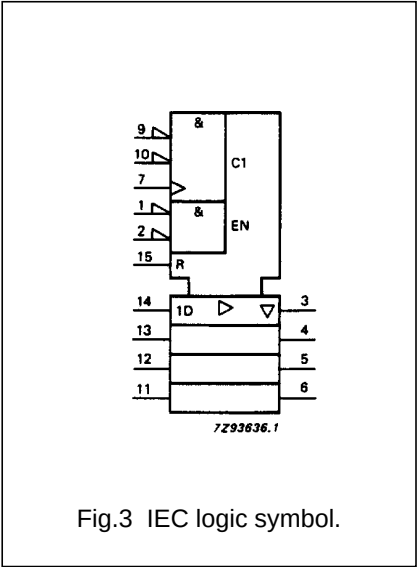
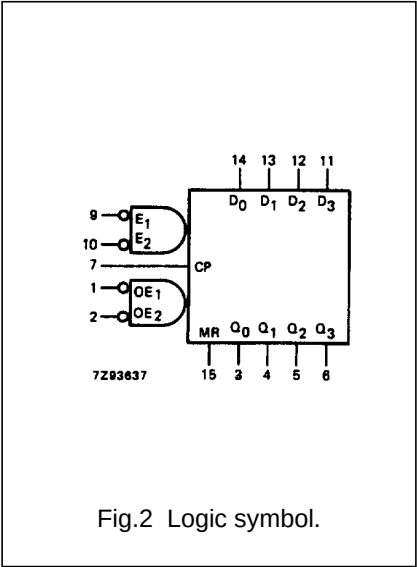
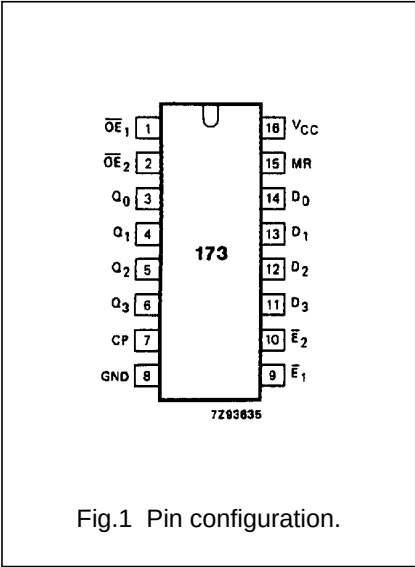
See "74HC/HCT/HCU/HCMOS Logic Package Information".

Quad D-type flip-flop; positive-edge trigger; 3-state

74HC/HCT173

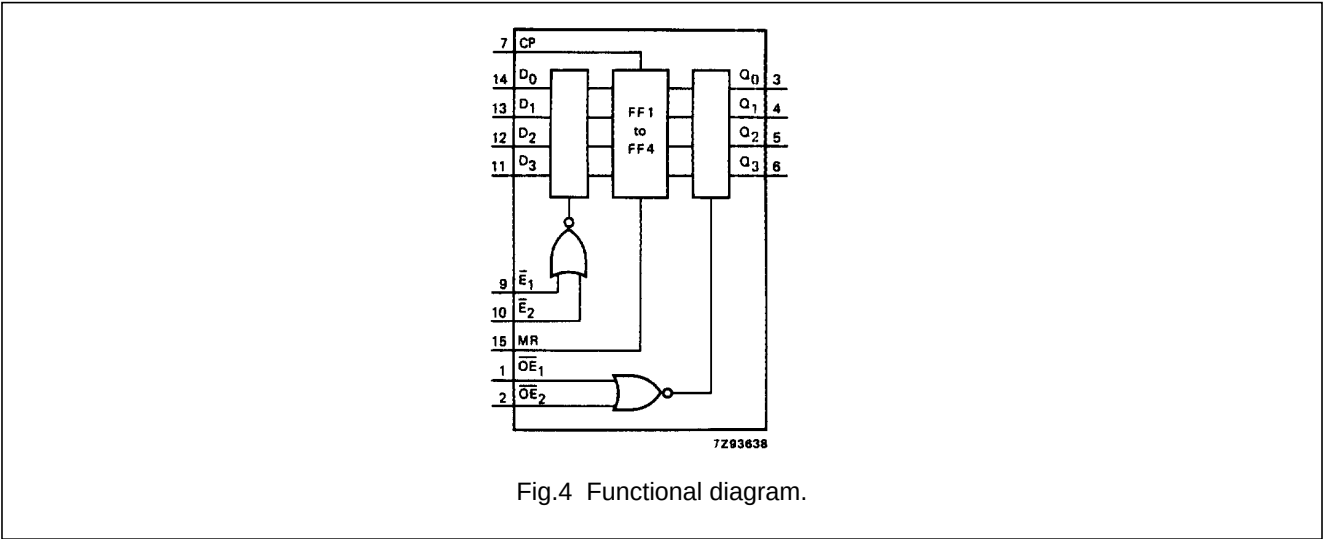
PIN DESCRIPTION

| PIN NO.        | SYMBOL                             | NAME AND FUNCTION                         |
|----------------|------------------------------------|-------------------------------------------|
| 1, 2           | $\overline{OE}_1, \overline{OE}_2$ | output enable input (active LOW)          |
| 3, 4, 5, 6     | $Q_0$ to $Q_3$                     | 3-state flip-flop outputs                 |
| 7              | CP                                 | clock input (LOW-to-HIGH, edge-triggered) |
| 8              | GND                                | ground (0 V)                              |
| 9, 10          | $\overline{E}_1, \overline{E}_2$   | data enable inputs (active LOW)           |
| 14, 13, 12, 11 | $D_0$ to $D_3$                     | data inputs                               |
| 15             | MR                                 | asynchronous master reset (active HIGH)   |
| 16             | $V_{CC}$                           | positive supply voltage                   |



Quad D-type flip-flop; positive-edge trigger; 3-state

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FUNCTION TABLE

| REGISTER OPERATING MODES | INPUTS |            |                  |                  |       | OUTPUTS          |  |  |  |
|--------------------------|--------|------------|------------------|------------------|-------|------------------|--|--|--|
|                          | MR     | CP         | $\overline{E}_1$ | $\overline{E}_2$ | $D_n$ | $Q_n$ (register) |  |  |  |
| reset (clear)            | H      | X          | X                | X                | X     | L                |  |  |  |
| parallel load            | L      | $\uparrow$ | L                | L                | L     | L                |  |  |  |
|                          | L      | $\uparrow$ | L                | L                | h     | H                |  |  |  |
| hold (no change)         | L      | X          | h                | X                | X     | $q_n$            |  |  |  |
|                          | L      | X          | X                | h                | X     | $q_n$            |  |  |  |

| 3-STATE BUFFER OPERATING MODES | INPUTS           |                   |                   | OUTPUTS |       |       |       |
|--------------------------------|------------------|-------------------|-------------------|---------|-------|-------|-------|
|                                | $Q_n$ (register) | $\overline{OE}_1$ | $\overline{OE}_2$ | $Q_0$   | $Q_1$ | $Q_2$ | $Q_3$ |
| read                           | L                | L                 | L                 | L       | L     | L     | L     |
|                                | H                | L                 | L                 | H       | H     | H     | H     |
| disabled                       | X                | H                 | X                 | Z       | Z     | Z     | Z     |
|                                | X                | X                 | H                 | Z       | Z     | Z     | Z     |

Notes

1.
- H = HIGH voltage level
- h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
- L = LOW voltage level
- L = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
- q = lower case letters indicate the state of the referenced input (or output)
- one set-up time prior to the LOW-to-HIGH CP transition
- X = don't care
- Z = high impedance OFF-state
- $\uparrow$  = LOW-to-HIGH CP transition

## Quad D-type flip-flop; positive-edge trigger; 3-state

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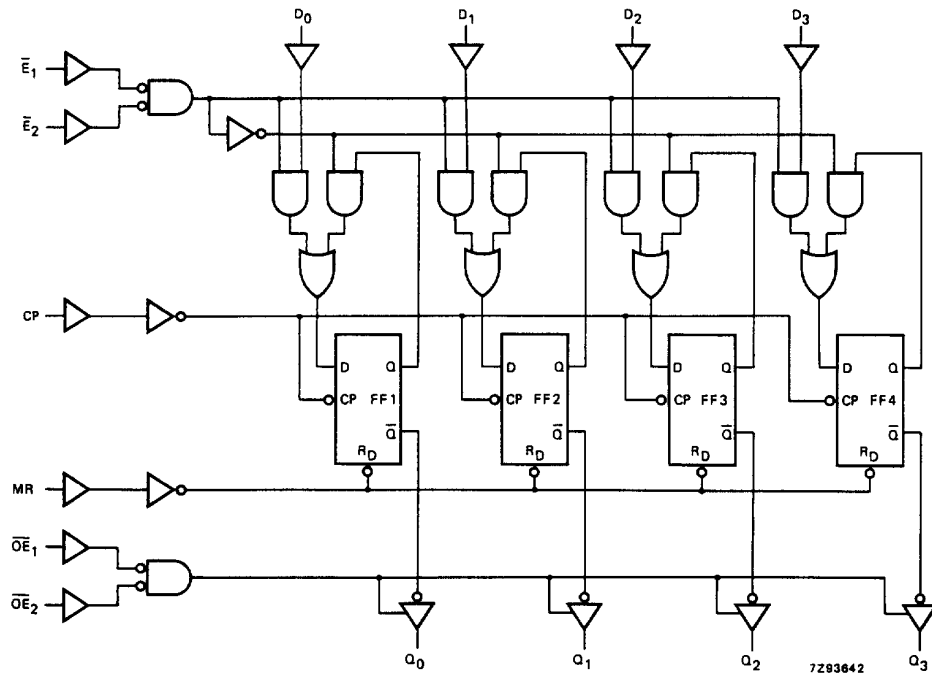


Fig.5 Logic diagram.

## Quad D-type flip-flop; positive-edge trigger; 3-state

## 74HC/HCT173

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I<sub>CC</sub> category: MSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

| SYMBOL                              | PARAMETER                                                          | T <sub>amb</sub> (°C) |                |                 |                 |                 |                 |                 | UNIT | TEST CONDITIONS        |           |
|-------------------------------------|--------------------------------------------------------------------|-----------------------|----------------|-----------------|-----------------|-----------------|-----------------|-----------------|------|------------------------|-----------|
|                                     |                                                                    | 74HC                  |                |                 |                 |                 |                 |                 |      | V <sub>CC</sub><br>(V) | WAVEFORMS |
|                                     |                                                                    | +25                   |                |                 | −40 to +85      |                 | −40 to +125     |                 |      |                        |           |
|                                     |                                                                    | min.                  | typ.           | max.            | min.            | max.            | min.            | max.            |      |                        |           |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>CP to Q <sub>n</sub>                          |                       | 55<br>20<br>16 | 175<br>35<br>30 |                 | 220<br>44<br>37 |                 | 265<br>53<br>45 | ns   | 2.0<br>4.5<br>6.0      | Fig.6     |
| t <sub>PHL</sub>                    | propagation delay<br>MR to Q <sub>n</sub>                          |                       | 44<br>16<br>13 | 150<br>30<br>26 |                 | 190<br>38<br>33 |                 | 225<br>45<br>38 | ns   | 2.0<br>4.5<br>6.0      | Fig.7     |
| t <sub>PZH</sub> / t <sub>PZL</sub> | 3-state output enable time<br>$\overline{OE}_n$ to Q <sub>n</sub>  |                       | 52<br>19<br>15 | 150<br>30<br>26 |                 | 190<br>38<br>33 |                 | 225<br>45<br>38 | ns   | 2.0<br>4.5<br>6.0      | Fig.8     |
| t <sub>PHZ</sub> / t <sub>PLZ</sub> | 3-state output disable time<br>$\overline{OE}_n$ to Q <sub>n</sub> |                       | 52<br>19<br>15 | 150<br>30<br>26 |                 | 190<br>38<br>33 |                 | 225<br>45<br>38 | ns   | 2.0<br>4.5<br>6.0      | Fig.8     |
| t <sub>THL</sub> / t <sub>TLH</sub> | output transition time                                             |                       | 14<br>5<br>4   | 60<br>12<br>10  |                 | 75<br>15<br>13  |                 | 90<br>18<br>15  | ns   | 2.0<br>4.5<br>6.0      | Fig.6     |
| t <sub>w</sub>                      | clock pulse width<br>HIGH or LOW                                   | 80<br>16<br>14        | 14<br>5<br>4   |                 | 100<br>20<br>17 |                 | 120<br>24<br>20 |                 | ns   | 2.0<br>4.5<br>6.0      | Fig.6     |
| t <sub>w</sub>                      | master reset pulse<br>width; HIGH                                  | 80<br>16<br>14        | 14<br>5<br>4   |                 | 100<br>20<br>17 |                 | 120<br>24<br>20 |                 | ns   | 2.0<br>4.5<br>6.0      | Fig.7     |
| t <sub>rem</sub>                    | removal time<br>MR to CP                                           | 60<br>12<br>10        | −8<br>−3<br>−2 |                 | 75<br>15<br>13  |                 | 90<br>18<br>15  |                 | ns   | 2.0<br>4.5<br>6.0      | Fig.7     |
| t <sub>su</sub>                     | set-up time<br>$\overline{E}_n$ to CP                              | 100<br>20<br>17       | 33<br>12<br>10 |                 | 125<br>25<br>21 |                 | 150<br>30<br>26 |                 | ns   | 2.0<br>4.5<br>6.0      | Fig.9     |
| t <sub>su</sub>                     | set-up time<br>D <sub>n</sub> to CP                                | 60<br>12<br>10        | 17<br>6<br>5   |                 | 75<br>15<br>13  |                 | 90<br>18<br>15  |                 | ns   | 2.0<br>4.5<br>6.0      | Fig.9     |

## Quad D-type flip-flop; positive-edge trigger; 3-state

## 74HC/HCT173

| SYMBOL           | PARAMETER                         | T <sub>amb</sub> (°C) |                 |      |                 |      |                 |      | UNIT | TEST CONDITIONS        |           |
|------------------|-----------------------------------|-----------------------|-----------------|------|-----------------|------|-----------------|------|------|------------------------|-----------|
|                  |                                   | 74HC                  |                 |      |                 |      |                 |      |      | V <sub>CC</sub><br>(V) | WAVEFORMS |
|                  |                                   | +25                   |                 |      | −40 to +85      |      | −40 to +125     |      |      |                        |           |
|                  |                                   | min.                  | typ.            | max. | min.            | max. | min.            | max. |      |                        |           |
| t <sub>h</sub>   | hold time<br>E <sub>n</sub> to CP | 0<br>0<br>0           | −17<br>−6<br>−5 |      | 0<br>0<br>0     |      | 0<br>0<br>0     |      | ns   | 2.0<br>4.5<br>6.0      | Fig.9     |
| t <sub>h</sub>   | hold time<br>D <sub>n</sub> to CP | 1<br>1<br>1           | −11<br>−4<br>−3 |      | 1<br>1<br>1     |      | 1<br>1<br>1     |      | ns   | 2.0<br>4.5<br>6.0      | Fig.9     |
| f <sub>max</sub> | maximum clock pulse<br>frequency  | 6.0<br>30<br>35       | 26<br>80<br>95  |      | 4.8<br>24<br>28 |      | 4.0<br>20<br>24 |      | MHz  | 2.0<br>4.5<br>6.0      | Fig.6     |

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Quad D-type flip-flop; positive-edge trigger; 3-state

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74HC/HCT173

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**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

| INPUT                              | UNIT LOAD COEFFICIENT |
|------------------------------------|-----------------------|
| $\overline{OE}_1, \overline{OE}_2$ | 0.50                  |
| MR                                 | 0.60                  |
| $\overline{E}_1, \overline{E}_2$   | 0.40                  |
| D <sub>n</sub>                     | 0.25                  |
| CP                                 | 1.00                  |

## Quad D-type flip-flop; positive-edge trigger; 3-state

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## AC CHARACTERISTICS FOR 74HCT

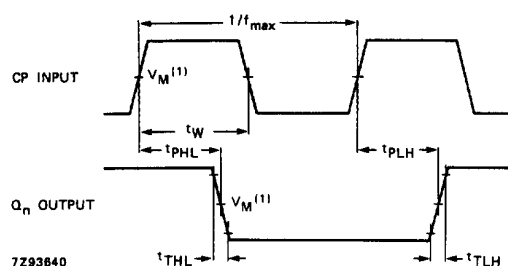
GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

| SYMBOL                              | PARAMETER                                                        | T <sub>amb</sub> (°C) |      |      |            |      |             |      | UNIT | TEST CONDITIONS        |           |
|-------------------------------------|------------------------------------------------------------------|-----------------------|------|------|------------|------|-------------|------|------|------------------------|-----------|
|                                     |                                                                  | 74HCT                 |      |      |            |      |             |      |      | V <sub>CC</sub><br>(V) | WAVEFORMS |
|                                     |                                                                  | +25                   |      |      | −40 to +85 |      | −40 to +125 |      |      |                        |           |
|                                     |                                                                  | min.                  | typ. | max. | min.       | max. | min.        | max. |      |                        |           |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>CP to Q <sub>n</sub>                        |                       | 20   | 40   |            | 50   |             | 60   | ns   | 4.5                    | Fig.6     |
| t <sub>PHL</sub>                    | propagation delay<br>MR to Q <sub>n</sub>                        |                       | 20   | 37   |            | 46   |             | 56   | ns   | 4.5                    | Fig.7     |
| t <sub>PZH</sub> / t <sub>PZL</sub> | 3-state output enable time<br>OE <sub>n</sub> to Q <sub>n</sub>  |                       | 20   | 35   |            | 44   |             | 53   | ns   | 4.5                    | Fig.8     |
| t <sub>PHZ</sub> / t <sub>PLZ</sub> | 3-state output disable time<br>OE <sub>n</sub> to Q <sub>n</sub> |                       | 19   | 30   |            | 38   |             | 45   | ns   | 4.5                    | Fig.8     |
| t <sub>THL</sub> / t <sub>TLH</sub> | output transition time                                           |                       | 5    | 12   |            | 15   |             | 19   | ns   | 4.5                    | Fig.6     |
| t <sub>W</sub>                      | clock pulse width<br>HIGH or LOW                                 | 16                    | 7    |      | 20         |      | 24          |      | ns   | 4.5                    | Fig.6     |
| t <sub>W</sub>                      | master reset pulse<br>width; HIGH                                | 15                    | 6    |      | 19         |      | 22          |      | ns   | 4.5                    | Fig.7     |
| t <sub>rem</sub>                    | removal time<br>MR to CP                                         | 12                    | −2   |      | 15         |      | 18          |      | ns   | 4.5                    | Fig.7     |
| t <sub>su</sub>                     | set-up time<br>E <sub>n</sub> to CP                              | 22                    | 13   |      | 28         |      | 33          |      | ns   | 4.5                    | Fig.9     |
| t <sub>su</sub>                     | set-up time<br>D <sub>n</sub> to CP                              | 12                    | 7    |      | 15         |      | 18          |      | ns   | 4.5                    | Fig.9     |
| t <sub>h</sub>                      | hold time<br>E <sub>n</sub> to CP                                | 0                     | −6   |      | 0          |      | 0           |      | ns   | 4.5                    | Fig.9     |
| t <sub>h</sub>                      | hold time<br>D <sub>n</sub> to CP                                | 0                     | −3   |      | 0          |      | 0           |      | ns   | 4.5                    | Fig.9     |
| f <sub>max</sub>                    | maximum clock pulse<br>frequency                                 | 30                    | 80   |      | 24         |      | 20          |      | MHz  | 4.5                    | Fig.6     |

# Quad D-type flip-flop; positive-edge trigger; 3-state

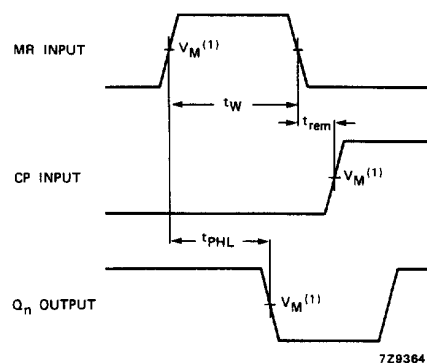
74HC/HCT173

## AC WAVEFORMS



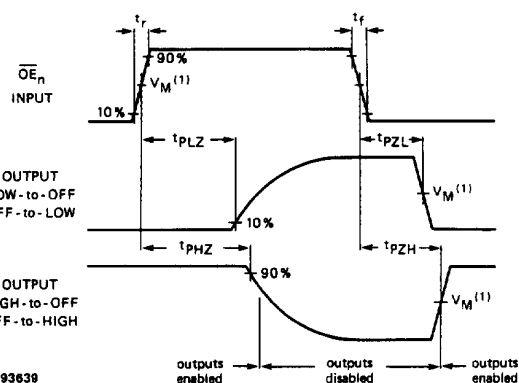
- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

Fig.6 Waveforms showing the clock (CP) to output ( $Q_n$ ) propagation delays, the clock pulse width, the output transition times and the maximum clock pulse frequency.



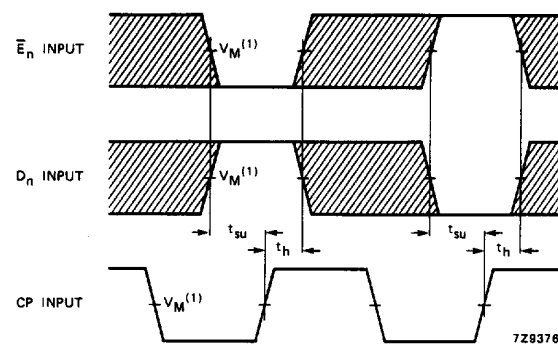
- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

Fig.7 Waveforms showing the master reset (MR) pulse width, the master reset to output ( $Q_n$ ) propagation delays and the master reset to clock (CP) removal time.



- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

Fig.8 Waveforms showing the 3-state enable and disable times.



The shaded areas indicate when the input is permitted to change for predictable output performance.

- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

Fig.9 Waveforms showing the data set-up and hold times from input ( $E_n$ ,  $D_n$ ) to clock (CP).

## PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".